REMARKS

New claims 44-48 have been added. Claims 1-48 are now pending in this application.

Reconsideration of the application is earnestly requested. The Examiner is thanked for the telephone interview of February 6, 2007.

The Office Action has allowed claims 4, 14, 15, 19, 20, 24, 25, 29 and 30. Claims 1-3, 5-13, 16-18, 21-23, 26-28, 31, and 32 have been rejected under 35 U.S.C. 103(a) as being unpatentable over some combination of *LaBerge* (U.S. Pat. No. 6,108,778) or *Lange* (U.S. Pat. No. 6,055,598). Although the Examiner's arguments have been carefully considered, Applicant respectfully traverses these rejections as explained below.

The Present Invention

The instant application points out at page 1, final paragraph, that conventional reset techniques perform a system-wide reset, placing all components into a known state. But, system-wide resets are unnecessarily disruptive. The present invention addresses this problem by providing a bus bridge device and associated method that handles a reset of components only on a first side of a bus bridge while the second side remains operating freely and without adversely affecting the second side. (See page 3, first paragraph; page 6, lines 15-17; and page 12, lines 14-17.) In other words, the first side of the bridge may be reset independently of the second side of the bridge.

The Cited Art Distinguished

By contrast, *LaBerge* discloses quite clearly a conventional reset technique that performs a system-wide reset. In other words, the disclosure of *LaBerge* is nothing more than the prior art described in the background of the instant application upon which the present invention improves. *LaBerge* discloses at column 1, lines 27-43 that the processor and all other computer system components are all reset. Column 4, lines 3-9 disclose that the reset command instructs all components (on both sides of bridge 50) of the system to reset. Further disclosure supporting Applicant's assertion that *LaBerge* requires that all component of the system be reset is found at column 4, lines 38-50 and at column 6, lines 13-19.

Claim 1

Claim 1 as amended now requires:

> receiving a reset signal at the bus bridge, the reset signal associated with a reset of the slave component and not being associated with the master component
>
> and
>
> resetting said slave component and not resetting said master component.

LaBerge cannot disclose these steps because the entire disclosure of *LaBerge* discusses resetting all components of the entire computer system on both sides of the bridge, whereas the above steps require that one side of the bridge, i.e., the side including the master component, is not reset.

Further, the Office action also alleges at page 3 lines 17-20 that *LaBerge* discloses allowing the master component to continue operating. But, claim 1 previously required (and still does):

> wherein responding with the master component bus protocol compliant signal *allows the master component to continue operating.*

But, *LaBerge* cannot disclose this limitation because all components are reset. If, for example, the processor (the master component) requests a reset, by definition it cannot continue operating because it has been reset!

For these reasons, it is respectfully requested that the rejection of claim 1 based upon *LaBerge* be withdrawn.

It is also submitted that the current amendments to claim 1 are fully supported by the specification and do not require a further search. For example, the term "bus protocols" in the last line of claim 1 has been replaced with "the master component bus protocol." Presumably, both protocols present in *LaBerge* were considered for the rejection and now the claim simply makes it clear that reference to the "master component bus protocol" is appropriate. Claim 1 now also requires that the slave component be reset. It is inherent in the claim before amendment that the slave component is reset because the claim previously required a reset signal associated with a reset of the slave component. Finally, claim 1 now requires that the reset signal is not associated with the master component and that the master component is not reset. Applicant points out that the specification makes quite clear that the nature of the invention is that one side of the bus is reset independently of the other side. Because the Patent Office is obligated to search features that Applicant might reasonably be expected to claim, it is submitted that no further search is required for this added limitation of claim 1. In any case, claim 1 as filed required that the master component continues operating which implies that it is not reset.

Claim 11

Claim 11 has been amended to more clearly point out the steps that are occurring in the claim; no new matter has been added and no further search is required.

Claim 11 now requires:

> receiving a reset signal on a first side of the bus bridge and not on a second side of said bus bridge;
>
> resetting a first component associated with the first side of said bus bridge and not resetting a second side of said bus bridge.

As discussed above, claim 11 requires that one side of a bus bridge is reset while the second side is not reset. *LaBerge* clearly discloses that both sides of its disclosed bridge receive a reset signal and that both sides must be reset as part of a system-wide reset.

For these reasons, it is respectfully requested that the rejection of claim 11 based upon *LaBerge* be withdrawn.

The above amendments to claim 11 are supported in the specification and do not require further search for the same reasons as discussed above with respect to claim 1.

Claim 21

Claim 21 has been amended to more clearly point out the steps that are occurring in the claim; no new matter has been added and no further search is required.

Claim 21 now requires:

> a master interface reset input arranged to receive a reset communication and to generate a reset signal in order to reset a slave component;

a slave interface reset input that does not generate any signal to reset a master component while said slave component is being reset;

As discussed above, claim 21 now requires that a reset of the slave component on the first side of the bus bridge is independent of a master component on the second side. In other words, the second side with the master component is not reset while the slave component is reset. *LaBerge* clearly discloses that both sides of its disclosed bridge receive a reset signal and that both sides must be reset as part of a system-wide reset.

For these reasons, it is respectfully requested that the rejection of claim 21 based upon *LaBerge* be withdrawn.

The above amendments to claim 21 are supported in the specification and do not require further search for the same reasons as discussed above with respect to claim 1. For example, the added interface reset inputs are shown in Figure 4 at numerals 404 and 424.

Claim 31

Claim 31 has been amended to require all of the limitations of claim 1 and is submitted to be patentable for the same reasons as discussed above with respect to claim 1.

New claims 44-48

Claims 44-48 specifically require "wherein said received reset signal is not associated with a system-wide reset." *LaBerge* makes clear that the resets that are disclosed are each part of a system-wide reset that resets all components on both sides of the bus bridge. Because these claims require that the reset signal is not associated with a system-wide reset, it is submitted that *LaBerge* not only does not disclose the subject matter of these claims but also teaches away from these claims.

Reconsideration of this application and issuance of a Notice of Allowance at an early date are respectfully requested. If the Examiner believes a telephone conference would in any way expedite prosecution, please do not hesitate to telephone the undersigned at (612) 252-3330.

Respectfully submitted,
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